Amendments to the Claims

Please amend Claim(s) 1, 3, 6-9, 11, 13 and 14. Please add new Claim(s) 15-20. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Currently Amended) A method of digitally processing samples comprising:

reading the samples into a tapped delay chain;

processing samples from taps on the delay chain; and

in response to receiving a signal of completion of ~~subsequent to~~ a processing event, reducing the length of the delay chain by shifting samples rapidly ~~from~~ out of the delay chain at a higher output rate than an input rate of samples coming ~~in; and~~ into the delay chain. ~~and reducing the length of the delay chain.~~

2. (Original) The method of Claim 1 wherein the samples are from a data packet.

3. (Currently Amended) The method of Claim 2 wherein the data packet conforms to ~~802.11~~ a transmission system selected from the group of 802.11a, 802.11g and HIPERLAN/2 transmission systems ~~standards~~.

4. (Original) The method of Claim 3 wherein the event includes a synchronization of the data packet.

5. (Original) The method of Claim 4 wherein the delay chain comprises a plurality of pipelined registers.

6. (Currently Amended) The method of Claim 5 wherein the ~~method~~ reducing the length of the delay chain is performed ~~is repeated to further reduce the length of the delay chain~~ until a desired length of the delay chain is achieved.

7. (Currently Amended) The method of Claim 5 wherein reducing the length of the delay chain ~~is performed by~~ further includes bypassing empty registers[[;]].

8. (Currently Amended) A method of digitally processing samples of a data packet comprising:

reading the samples from a data packet into a tapped delay chain comprising a plurality of pipelined registers;

processing samples from taps on the delay chain to synchronize a data packet;

in response to receiving a signal of completion of ~~subsequent to~~ synchronization of the data packet, reducing the length of the delay chain by shifting samples rapidly out of ~~from~~ the delay chain at a higher output rate than an input rate of samples coming ~~in;~~ into the delay chain;

~~reducing the length of the delay chain by~~ bypassing empty registers; and

repeating the steps of ~~shifting samples rapidly and~~ reducing the length of the delay chain.

9. (Currently Amended) An apparatus comprising:

a pipeline of registers that store data samples;

logic circuitry which controls the output of each individual register from the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on a plurality of processing events of the apparatus.

10. (Original) An apparatus of Claim 9 wherein the data samples are from a data packet.

11. (Currently Amended) ~~An~~ The apparatus of Claim 10 data packet conforms to 802.11a, 802.11g and HIPERLAN/2 transmission systems standards.

12. (Original) An apparatus of Claim 11 further comprising a timing recovery module for synchronization of the data packet that initiates a transition in the processor.

13. (Currently Amended) An apparatus comprising:

a pipeline of registers that stores data samples of a data packet;

a timing recovery module for synchronization of the data packet that initiates a transition;

a logic circuitry which controls the output of each individual register from the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor having inputs from a timing recovery module for packet synchronization which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on a plurality of processing events of the apparatus.

14. (Currently Amended) An apparatus comprising:

means for reading data samples into a tapped delay chain;

means for processing data samples from taps on the delay chain;

means for reducing the length of the delay chain in response to receiving a signal of completion of a processing event. ~~shifting data samples rapidly from the delay chain at a higher rate than data samples coming in, and~~

~~means for reducing the length of the delay chain.~~

15. (New) Within a digital processor, a method of dynamically reducing a digital delay chain comprising:

providing a delay chain with an output rate higher than an input rate; and

shifting data samples out of the delay chain at the higher output rate while reading additional data samples into the input end of the delay chain at the input rate.

16. (New) The method of Claim 15 further comprising bypassing an empty portion of delay chain.

17. (New) The method of claim 15 performed in response to receiving a signal of completion of a processing event.

18. (New) The method of claim 17 wherein the data samples are from a data packet signal of completion of a processing event is a sync signal indicating synchronization of the data packet.

19. (New) The apparatus of Claim 9 wherein the processor is a state-machine.

20. (New) The apparatus of Claim 13 wherein the processor is a state-machine.